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10EC56

Fifth Semester B.E. Degree Examination, December 2012
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the nMOS fabrication process with neat diagram. **(10 Marks)**

b. Obtain the dc transfer characteristics of a CMOS inverter and mark all the region showing the status of PMOS and NMOS. **(10 Marks)**

2 a. Compare CMOS and bipolar technologies. **(04 Marks)**

b. Draw the circuit schematic and stick diagram of CMOS 2 input NAND gate. **(06 Marks)**

c. Draw the layout for the schematic shown in the Fig.Q.2(c). **(10 Marks)**

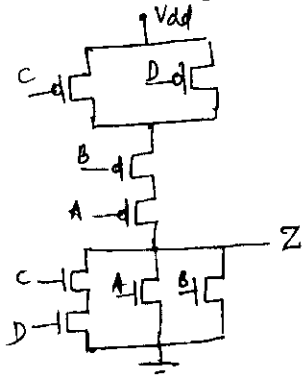

Fig.Q.2(c)

3 a. Explain the operation of CMOS dynamic logic. Also discuss the cascading problem of dynamic CMOS logic. **(10 Marks)**

b. Realize $Z = \overline{A(B+C)+DE}$ for clocked CMOS logic. **(05 Marks)**

c. Find the equation for the node voltages V_1, V_2, V_3 during logic "1" transfer, when each pass transistor is driving another pass transistor, as shown in Fig.Q.3(c). Assume threshold voltage of each transistor is V_{tn}. **(05 Marks)**

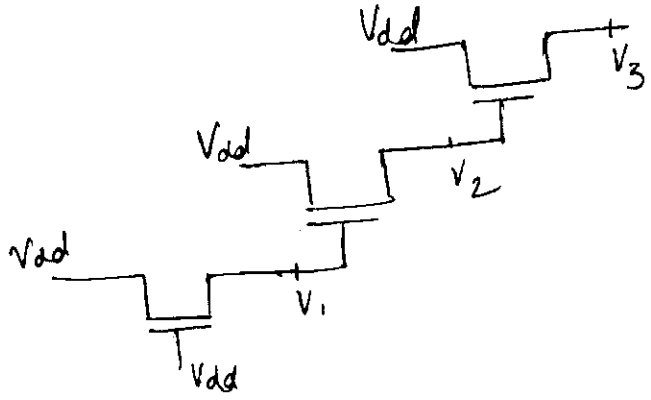

Fig.Q.3(c)

4 a. Find the scaling factors for:
   i) Channel Resistance Ron
   ii) Current density J. **(06 Marks)**
   b. Derive the equation for rise time and fall time for CMOS inverter. **(08 Marks)**
   c. Write a note on limitations of scaling. **(06 Marks)**

PART – B

5 a. Explain structured design of bus arbitration logic for n-line bus. **(10 Marks)**
   b. Explain dynamic 4-bit shift register using CMOS logic. **(10 Marks)**

6 a. Design 4-bit ALU to implement addition, subtraction, EXOR, EXNOR, OR and AND operations. **(10 Marks)**
   b. With the neat diagram, explain Braun array multiplier. **(10 Marks)**

7 a. Explain the working of three-transistor dynamic RAM cell. **(06 Marks)**
   b. Explain one transistor dynamic memory cell with schematic and stick diagram. **(06 Marks)**
   c. Discuss CMOS pseudo-static memory cell with stick diagram. **(08 Marks)**

8 a. Explain sensitized path-based testing for combinational logic. **(10 Marks)**
   b. Write a note on ground rules for successful design. **(10 Marks)**

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